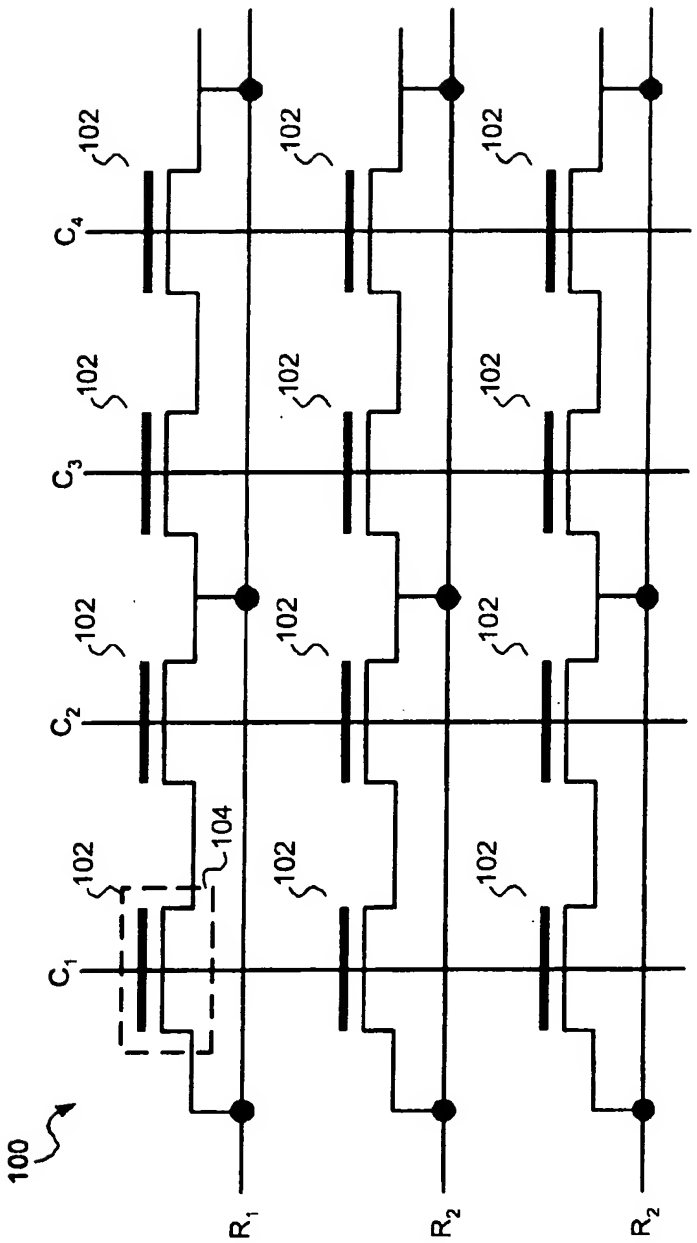

FIGURE 1

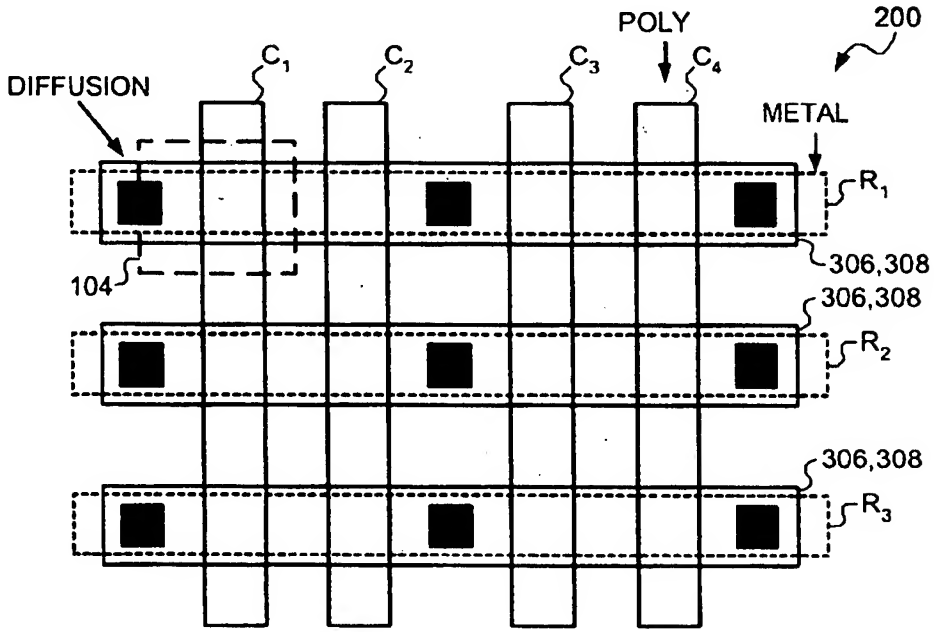
DIFFUSION
C1
C2
C3
POLY
C4
200
METAL
R1
306,308
104
306,308
R2
306,308
R3

FIGURE 2

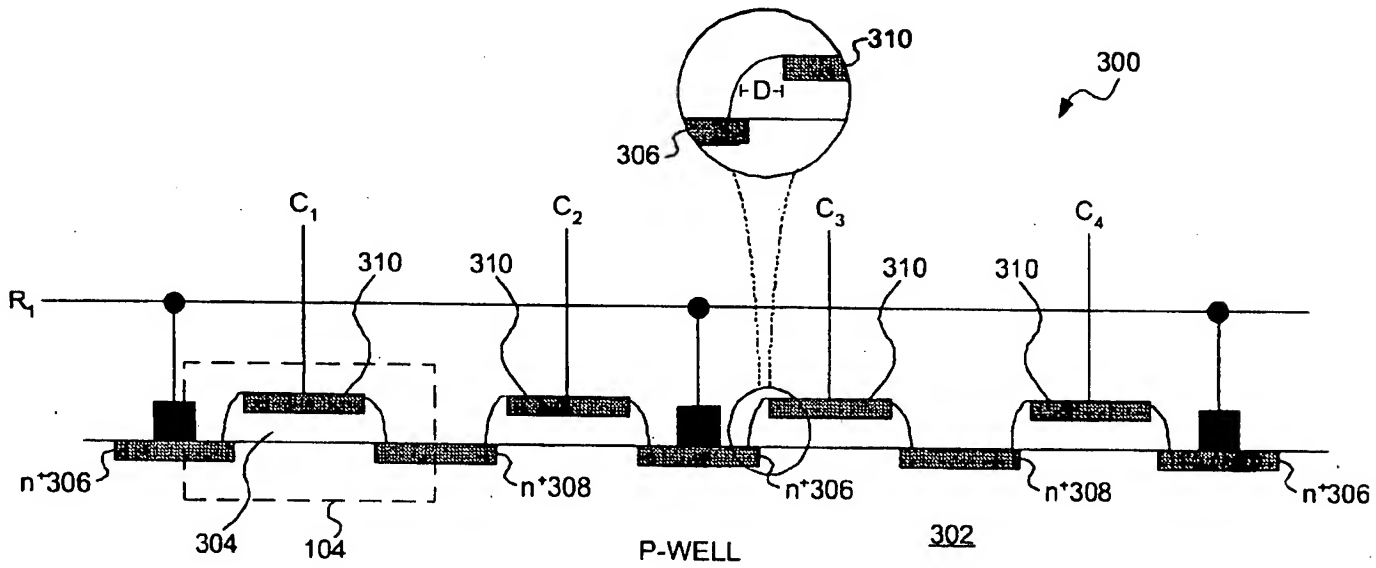
310
300
D
306
C1
C2
C3
C4
310
310
310
310
R1
n+306
n+308
n+306
n+308
n+306
304
104
P-WELL
302

FIGURE 3

		VBL (V)	VWL (V)	PROGRAM	
PROGRAM	SC/SR	8	0	YES	401
	SC/UR	8	8	NO	403
	UC/SR	3.3	0	NO	405
	UC/UR	3.3	8	NO	407
				ISENSE	
READ	SC/SR	1.8	0	YES	409
	SC/UR	1.8	1.8	NO	411
	UC/SR	0	0	NO	413
	UC/UR	0	1.8	NO	415

FIGURE 4

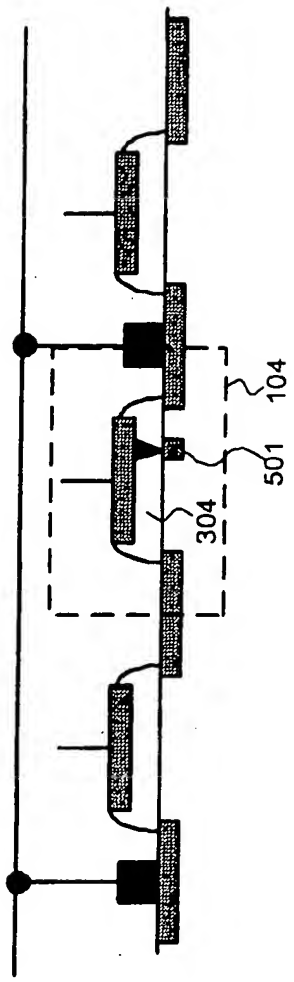

FIGURE 5

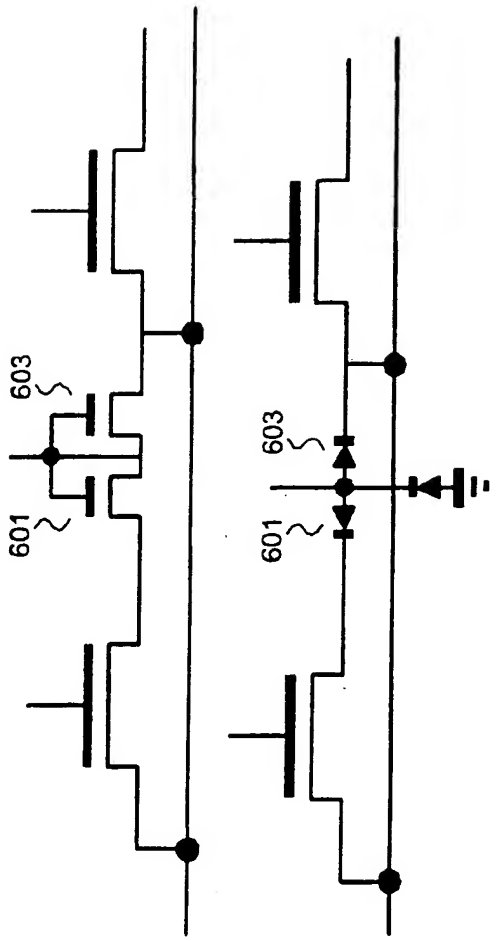

FIGURE 6

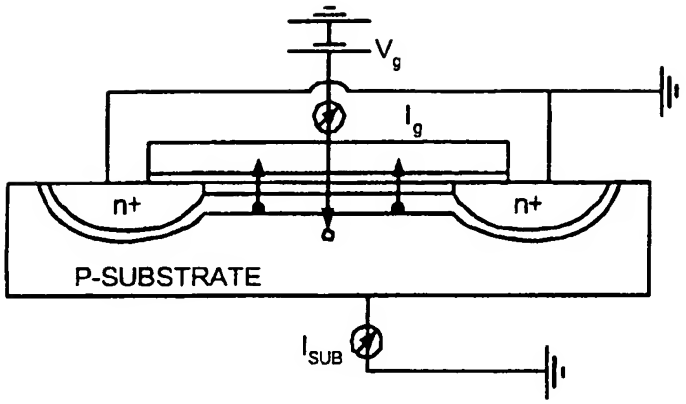

FIGURE 7

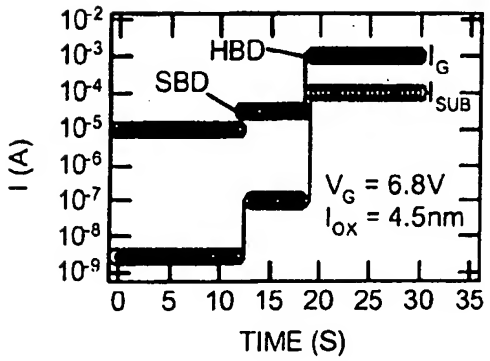

FIGURE 8

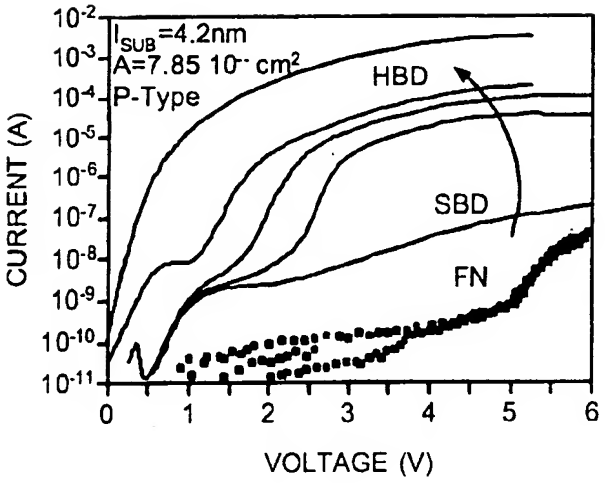
I_{SUB}=4.2nm
A=7.85 10⁻⁴ cm²
P-Type
HBD
SBD
FN
CURRENT (A)
VOLTAGE (V)
10⁻²
10⁻³
10⁻⁴
10⁻⁵
10⁻⁶
10⁻⁷
10⁻⁸
10⁻⁹
10⁻¹⁰
10⁻¹¹
0
1
2
3
4
5
6

FIGURE 9

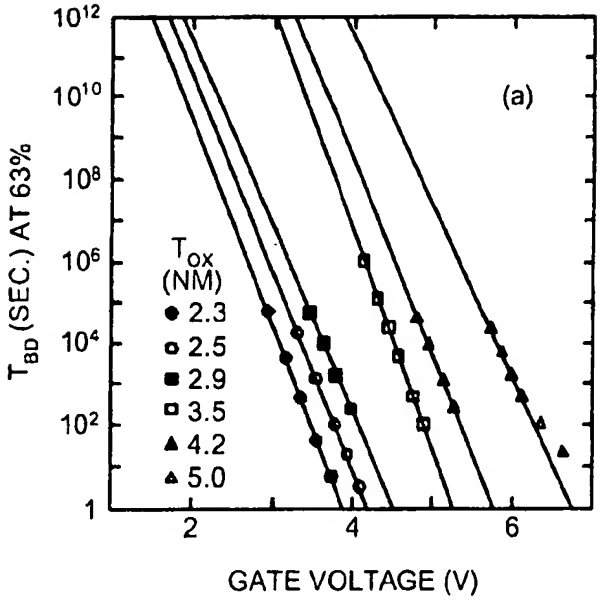
10^{12}
10^{10}
10^{8}
10^{6}
10^{4}
10^{2}
1
T_{BD} (SEC.) AT 63%
(a)
T_{ox} (NM)
2.3
2.5
2.9
3.5
4.2
5.0
2
4
6
GATE VOLTAGE (V)

FIGURE 10

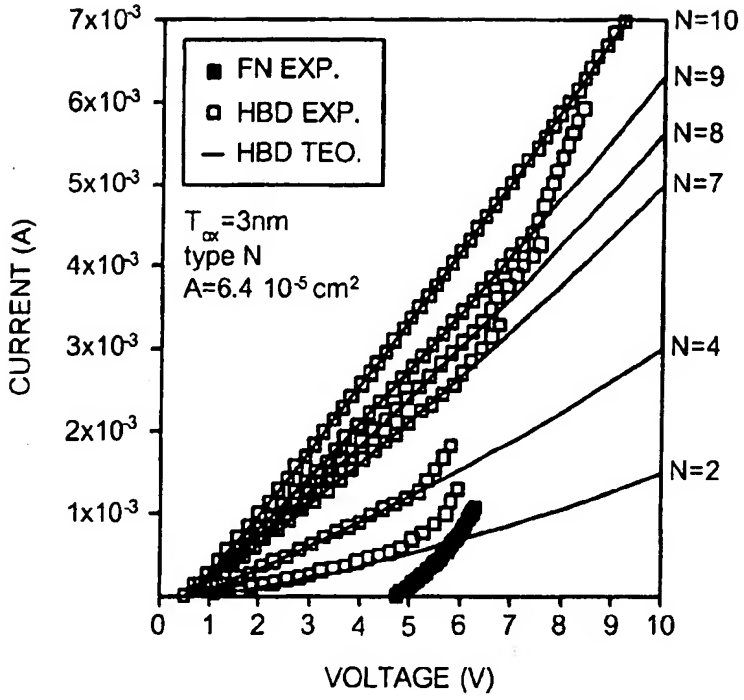
7x10-3
6x10-3
5x10-3
4x10-3
3x10-3
2x10-3
1x10-3
CURRENT (A)
FN EXP.
HBD EXP.
HBD TEO.
Tox=3nm
type N
A=6.4 10-5 cm2
N=10
N=9
N=8
N=7
N=4
N=2
0 1 2 3 4 5 6 7 8 9 10
VOLTAGE (V)

FIGURE 11

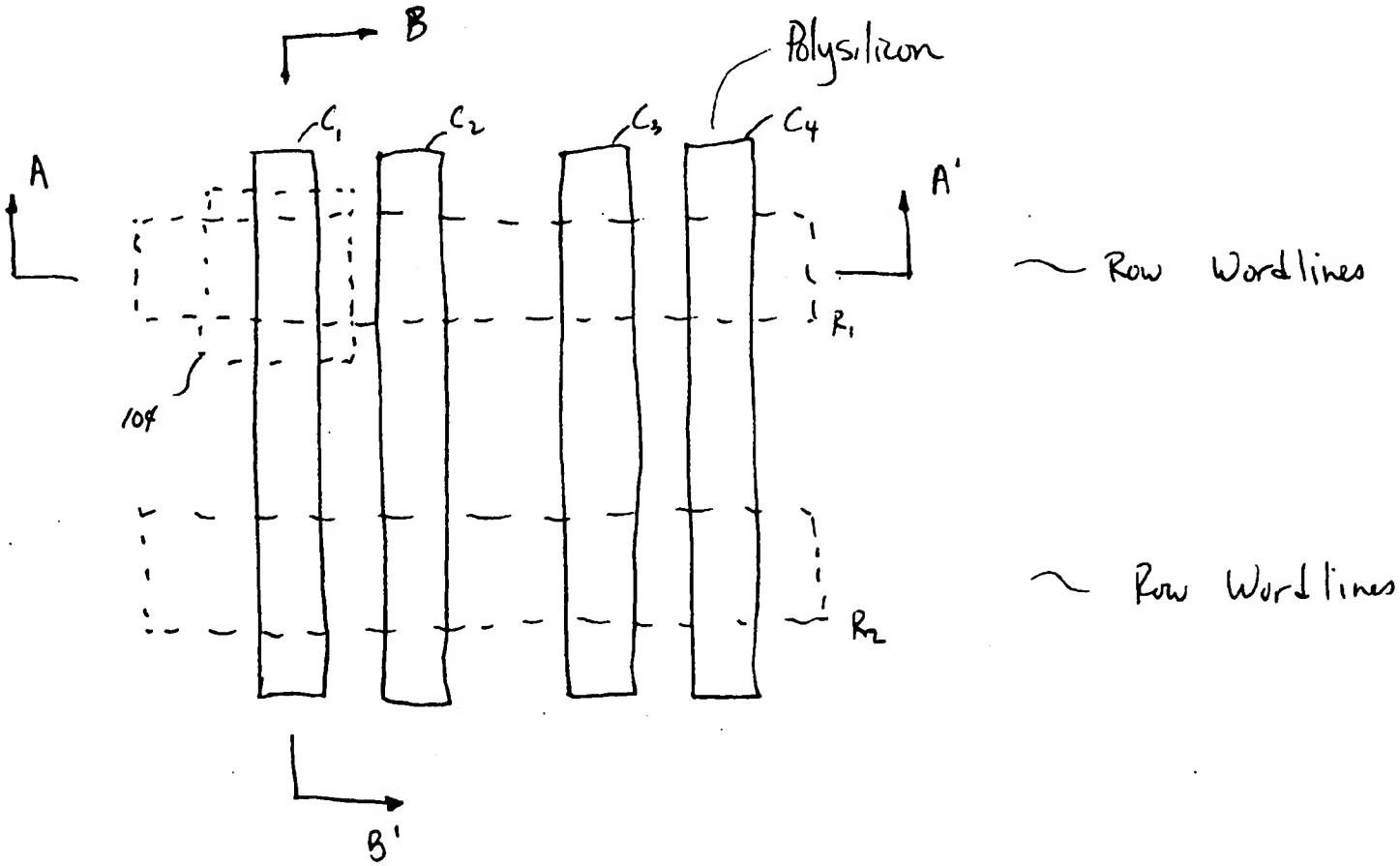
B
Polysilicon
C1
C2
C3
C4
A
A'
Row Wordlines
R1
10
R2
Row Wordlines
B'

Figure 12

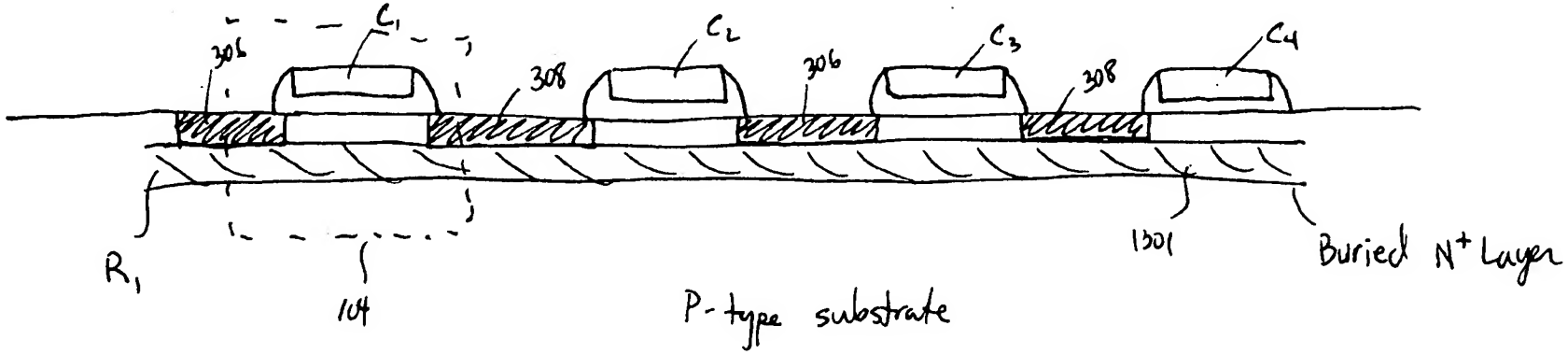
C1
C2
C3
C4
306
308
306
308
R1
104
P-type substrate
1301
Buried N+ Layer

Figure 13

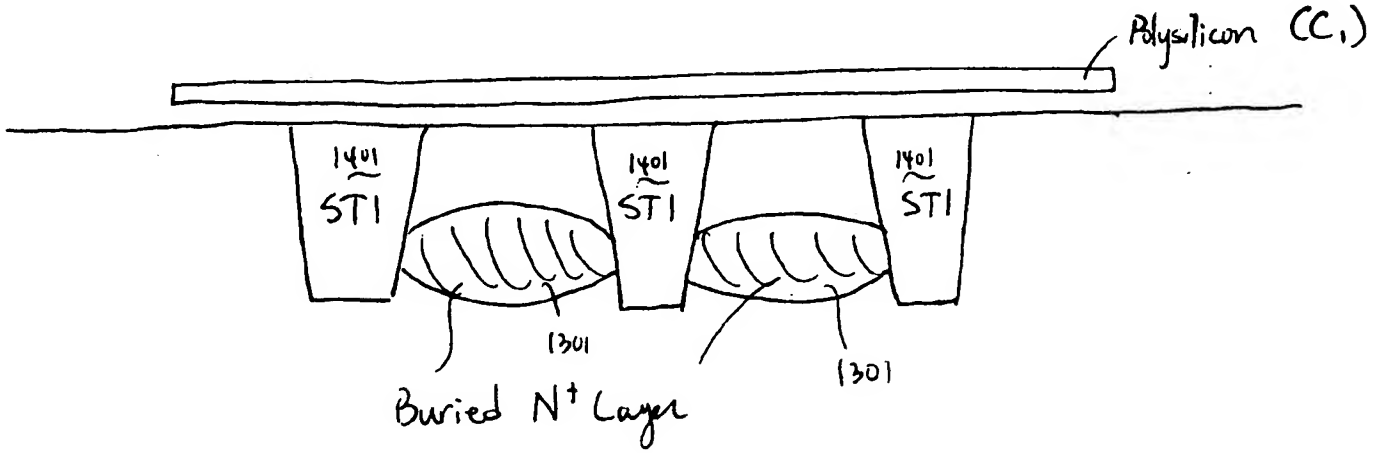
Polysilicon (C1)
1401
STI
1401
STI
1401
STI
1301
1301
Buried N+ Layer

Figure 14

		VBL (V)	VWL (V)	PROGRAM	
PROGRAM	SC/SR	V_{PP}	0	YES	401
	SC/UR	V_{PP}	Floating	NO	403
	UC/SR	< 0.5,	0	NO	405
	UC/UR	< 0.5,	Floating	NO	407
				ISENSE	
READ	SC/SR	V_{DD} or V_{CC}	0	YES	409
	SC/UR	V_{DD} or V_{CC}	V_{DD} or V_{CC}	NO	411
	UC/SR	0 or Float	0	NO	413
	UC/UR	0 or Float	V_{DD} or V_{CC}	NO	415

FIGURE 15

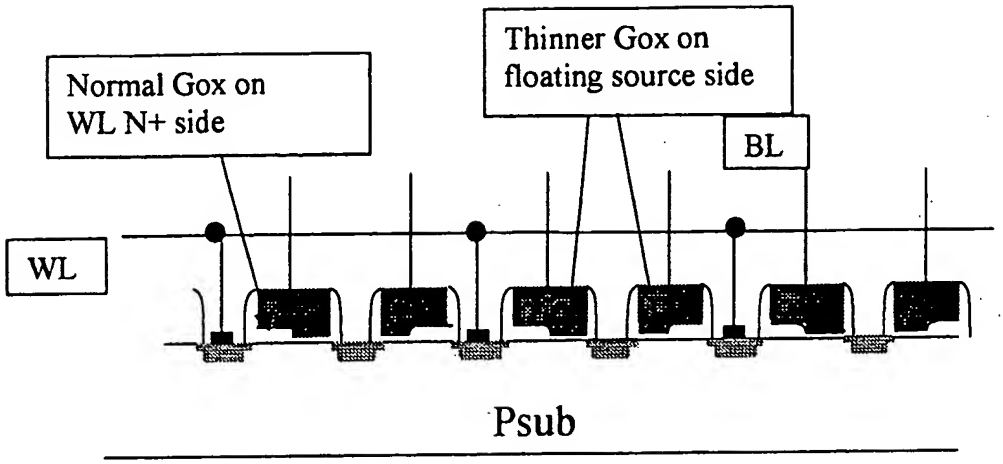
Normal Gox on
WL N+ side
Thinner Gox on
floating source side
BL
WL
Psub

Fig 16

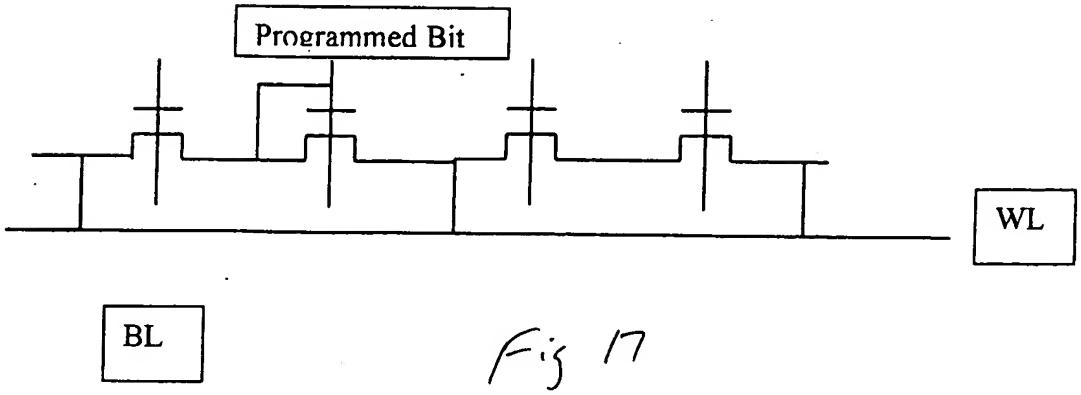
Programmed Bit
WL
BL

Fig 17

0.18um/0.13um XPM CX cell operation

		Vbl (V)	Vwl (V)	Program
Program	SB/SW	Vpp	0	Yes
	SB/UW	Vpp	PC to Vpp/2 and FL	No
	UB/SW	<0.5v	0	No
	UB/UW	<0.5v	PC to Vpp/2 and FL	No
				Isense
Read	SB/SW	Vdd or Vcc	0	Yes
	SB/UW	Vdd or Vcc	Vdd or Vcc	No
	UB/SW	0	0	No
	UB/UW	0	Vdd or Vcc	No

Vpp = 8~9V for Gox=32A (0.18um) or 5-7 for Gox=20A, or 3~4.5 V for 10-15A (5 to 10A thinner than ~~normal~~ standard Gate oxide).

Vdd = I/O Voltage 3.3V or 2.5V

Vcc=1.8V for 0.18um and 1.2V for 0.13um

Fig 18

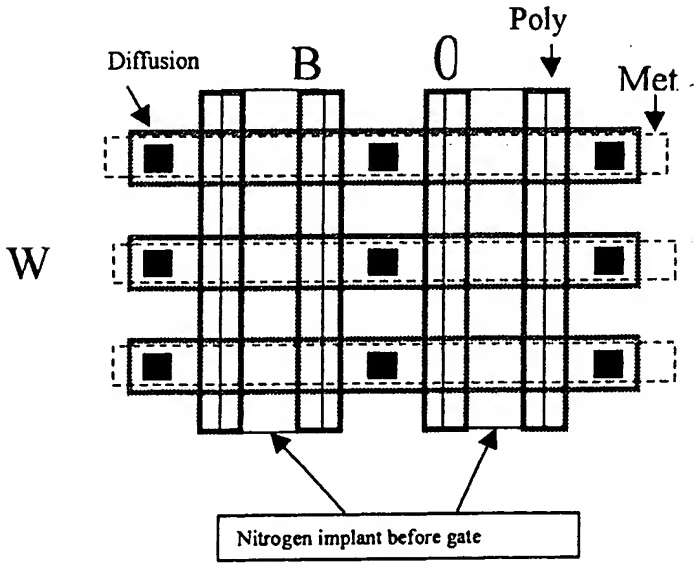

Fig 19

Step 1:

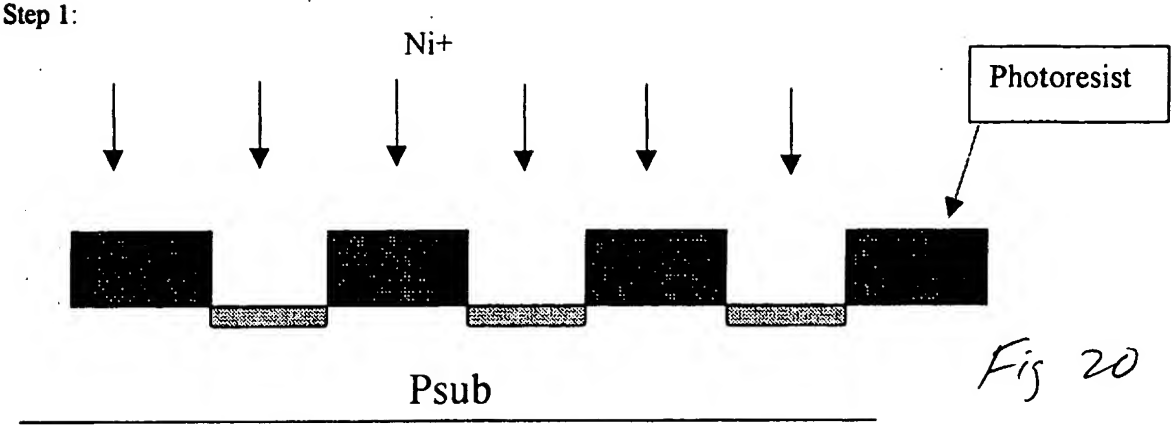

Fig 20

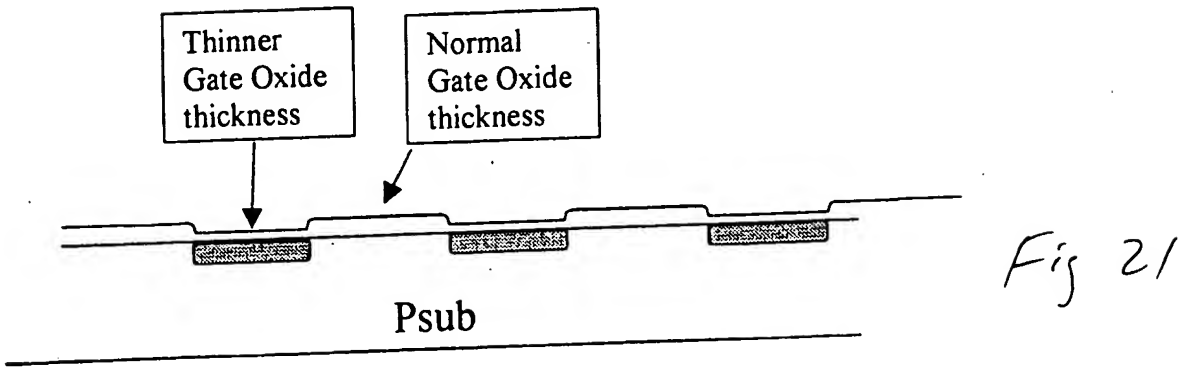

Fig 21

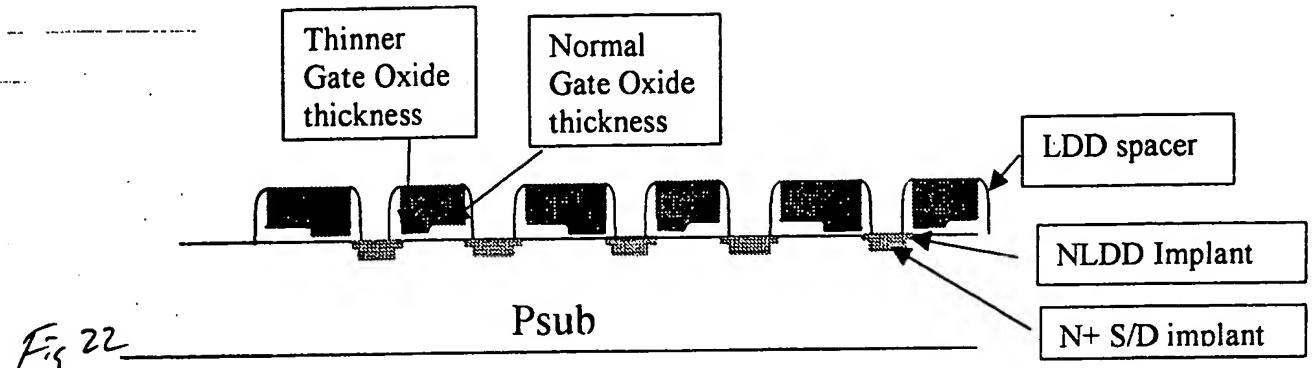

Fig 22

Fig 22

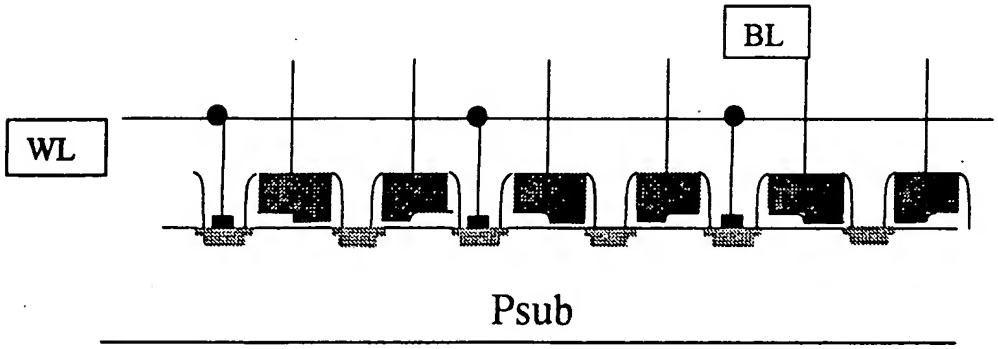

Fig 23

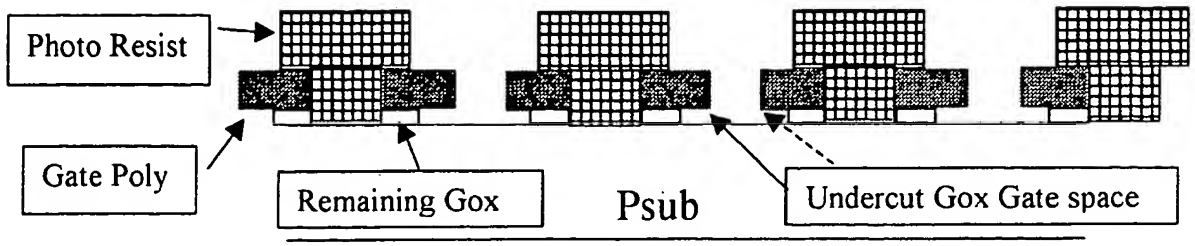
Photo Resist
Gate Poly
Remaining Gox
Psub
Undercut Gox Gate space

Fig. 24

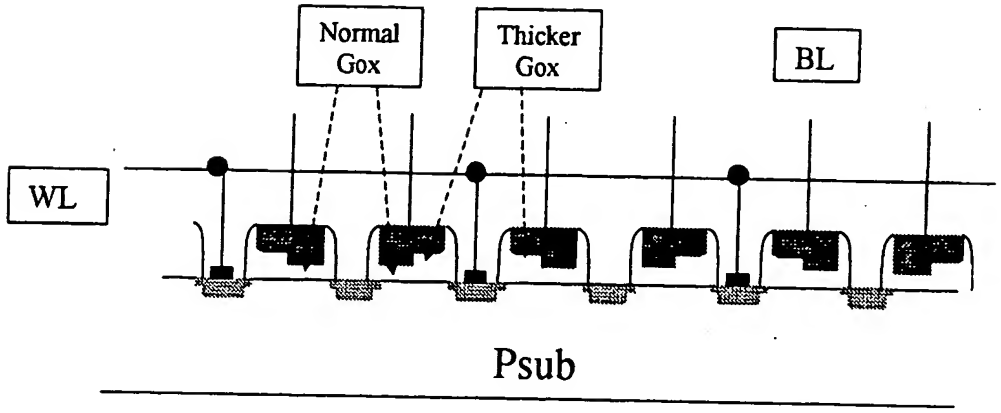
Normal Gox
Thicker Gox
BL
WL
Psub

Fig 25

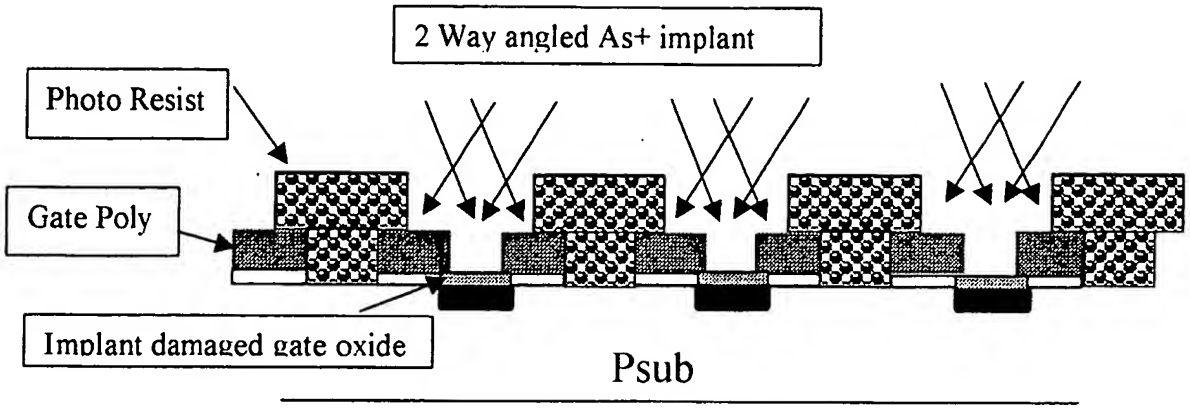
2 Way angled As+ implant
Photo Resist
Gate Poly
Implant damaged gate oxide
Psub

Fig 26

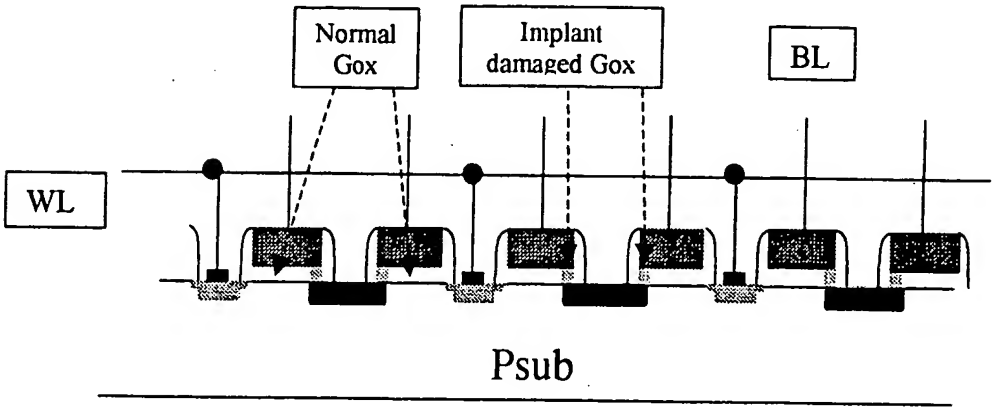
Normal Gox
Implant damaged Gox
BL
WL
Psub

Fig 27